Designing and Building Atlas

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http://www.cs.man.ac.uk/CCS/res/res62.htm#top

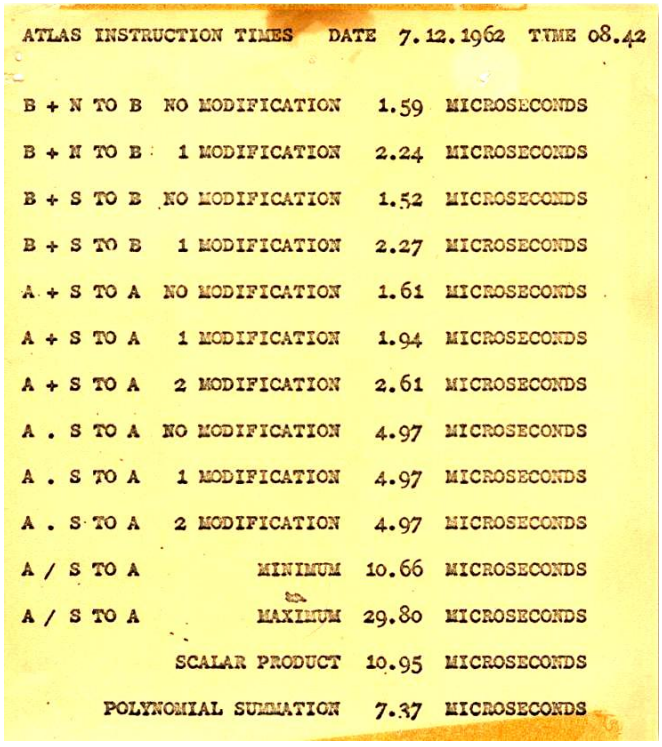
Following on from Simon Lavington's article on the politics of Atlas development in *Resurrection 61* (Spring 2013), we consider here the technical challenges in the design of such an advanced computer and consider how they were overcome. The Manchester Atlas operated from its inauguration day, 7th December 1962, to 30th September 1971 when it was closed down.

Introduction

The two prime movers in establishing the Atlas project were first, Sebastian de Ferranti, who supplied the money and took the risk in line with the Ferranti policy of being "First into the Future". A Ferranti leaflet dated November 1961 listed Ferranti products and this statement was printed on its front page. It certainly applied to computing and they had a good record in this respect for a number of other products dating from their start up as a company in 1882. The other was Professor Tom Kilburn who spearheaded the design and implementation. His belief in the project and his determination to see it through to a successful conclusion against considerable odds was remarkable. The decision to start the project was taken in late 1958 but the concepts originated from ideas and work already being undertaken by a small team at the University under Kilburn's direction and identified then as "Muse". Atlas started to run a computing service from the beginning of January 1963. There is little doubt that without the Ferranti collaboration Atlas would not have been built. Some senior people at the time commented that the whole of the UK would only need one Atlas, therefore there was no need to design and build it and the idea of buying American could be financially more attractive.

From the current situation in digital techniques with small mobile smart telephones and very capable tablets and laptop computers it is very difficult to appreciate the technical position as it was 50 years ago! Then there was a scarcity of storage, the equipment was physically large, constructional problems were difficult involving a lot of work by hand and there was only a limited interest because of cost and the difficulties of providing a satisfactory architecture with adequate performance.

The physical size of Atlas is immediately obvious from the photograph on the previous page, which shows part of the installation at the University. In the centre background two large cabinets can be seen and there were three more in this room. Additional cabinets for the magnetic drum memory, the power supply switching system and eight magnetic tape decks occupied an adjacent room. Yet another room housed peripheral equipment. The large physical size made it difficult to consider the use of a clock so the timing was implemented on an asynchronous basis. This too had problems, in particular selecting an event to activate when other requests can actually occur during the period used to determine the actual selection thus causing smaller pulse widths which may not be adequate to set flip-flops properly for example. This issue was dealt with by designing the mean time between failures for this situation to be the order of several months. The problem is described in more detail and in modern terms by David Kinniment [1]. Note also the three computer operators (replacing users) seated at desks with their own peripheral equipment linked into the machine. Atlas was able to multi-task in contrast to previous computers where one user only was in charge of the computer for a specified period. This meant that users now handed their problems over to computer service operators so that the users were no longer there when their problems ran. The job scheduling was determined by Atlas to balance its workload and minimise hold ups rather than a job being carried out at a specific time, though there may have been occasions when it was a requirement for users to be present.



ATLAS INSTRUCTION TIMES DATE 7.12.1962 TIME 08.42

B + N TO B	NO MODIFICATION	1.59	MICROSECONDS
B + N TO B	1 MODIFICATION	2.24	MICROSECONDS
B + S TO B	NO MODIFICATION	1.52	MICROSECONDS
B + S TO B	1 MODIFICATION	2.27	MICROSECONDS
A + S TO A	NO MODIFICATION	1.61	MICROSECONDS
A + S TO A	1 MODIFICATION	1.94	MICROSECONDS
A + S TO A	2 MODIFICATION	2.61	MICROSECONDS
A . S TO A	NO MODIFICATION	4.97	MICROSECONDS
A . S TO A	1 MODIFICATION	4.97	MICROSECONDS
A . S TO A	2 MODIFICATION	4.97	MICROSECONDS
A / S TO A	MINIMUM	10.66	MICROSECONDS
A / S TO A	MAXIMUM	29.80	MICROSECONDS
	SCALAR PRODUCT	10.95	MICROSECONDS
	POLYNOMIAL SUMMATION	7.37	MICROSECONDS

On the left we list the instruction times for a variety of different types of instruction. It is a copy of those printed out at 08:42 on the morning of inauguration day. The first four instructions are those associated with the B-arithmetic unit which operated on half-words (24 bits) and worked in a fixed point way. As in earlier machines an important function of the B-unit was also to provide the option of modifying any instruction address as that instruction is obeyed. There were 128 B-registers some of which had special organisational functions. The other eight instructions worked with the A-arithmetic unit which was a full-word unit with a double word length accumulator register to provide floating point arithmetic including multiplication and division facilities. As each of these units was distinct it was possible to obey B-instructions during the time that the A-unit was still obeying longer instructions such as multiplication or division. This process is termed overlap and in essence, since it also involves extracting instructions to obey before the previous instruction is complete, it is really the start of pipelining but that technique was not pursued very far in Atlas.

[1] *Synchronization and Arbitration in Digital systems. D. Kinniment. John Wiley& Sons Ltd 2007*

Features
The aim of the Atlas design was to provide a step function increase in throughput for user jobs, for example equivalent to 60 to 70 Mercury computers. Note that a single Mercury provided the University of Manchester computing service from February 1958 to January 1963 and was also used by others. The full potential of Atlas took about a year to achieve since for example, the peripheral equipment only arrived during a period of three months after the inauguration. Also there was the Supervisor software to develop fully from its initial state and there were language compilers to provide. Atlas was also running a computing service based on Mercury Autocode to simplify the transfer of user's earlier work to the Atlas computer.

To get the magnitude of performance required the computer had to be completely parallel in operation in contrast to previous machines designed at Manchester which were mainly serial in operation. This meant a significant increase in equipment and therefore cost too. With Mercury costing say £150K and Atlas £3,000K this was a 20 times increase in cost. Note however that Atlas provided a factor of 60 times improvement in throughput so that cost per smaller job done is reduced by a factor approaching three and of course Atlas made feasible the execution of much larger jobs in an acceptable time.

Multi-tasking also helped to improve job throughput and this is explained simply as follows. On Mercury a user would book a period of use, first spend some time inputting data, followed by computing time and then a time for getting the requisite output. In practice these three time slots, of input, compute, then output would differ from problem to problem but since the peripheral equipments were relatively slow I am going to assume all three times were identical for simplicity. The processor time the computer needed to either control the acceptance of data from or provide data to the peripherals was quite small so that it was mainly idle during the input and output time slot times which were defined by the amount of data involved and the peripheral speed of operation. If during the computation time the computer could be arranged to input the data for the next job to be run and also output the data for the previous job run then the computation time for that user would increase slightly but now computation could be carried out for most of the time available and thus throughput improved. Externally it appeared that the tasks of input, computation and output were all being carried out in parallel but the computer was essentially time sharing its operation for the initiation and control of these activities in sequence.

Ideally in a computer one would like the main memory to be large and provide random access but certainly 50 years ago this was not technically feasible and systems with the best performance were small and expensive. Here it was intended to use ferrite cores for the two microsecond cycle RAM and partially switch the cores for the faster B-store but considerable work was needed to provide this capability. In previous machines such as the Mk1 and Mercury there was a compromise with the available RAM being backed up by a slower access time magnetic drum of larger capacity which was cheaper to provide. The difficulty for the user was that they had to arrange transfers of information between the two levels of storage in such a way that a significant amount of time was not wasted. In Atlas such transfers were arranged efficiently by the computer with the provision of extra hardware and software providing autonomous block/page transfers of 512 words via DMA. To create some space in the RAM a suitable block had to be transferred back to the drum, i.e. the one least likely to be needed for some time. Statistics about the use of all the blocks in the RAM had to be maintained to enable the computer to make this selection and

this was done via a piece of software which was called the “learning program”. This system arrangement at the time was known as One Level Storage and essentially it converted user addresses within a large range to be available from a real physical address in the RAM. It also enabled protection to be provided which prevented one program interfering with another. This was the start of the Virtual Memory concept now available in modern computers.

The organisational software for the one level store was provided in a fixed store i.e. a ROM which was also linked to a small RAM providing some working space for this software and the combination was termed the Private Store in Atlas. This private store was not available to normal users and so provided added security to the organisational software. It also contained other software, such as test programs, peripheral drivers, and extensions to the basic instruction set which were called “Extracodes”. Extracodes were essentially subroutines to carry out more complex operations but the entry to the subroutine and the return from it could occur automatically with the help of B-register 121. To facilitate the operation there were two Control registers the MAIN control provided by B-register 127 for normal instructions and EXTRACODE control in B-register 126 to step through the subroutine instructions for Extracode operation. There was also a third Control register in B-register 125 called INTERUPT control which was used to help determine the source of any interrupt signal in the machine which would mainly arise from peripheral equipment requiring attention but also included various error conditions too. Such signals were given a priority of response depending on their ability to cope with time delay and in some cases peripheral equipment could be temporarily halted in operation. It was possible to determine which one of up to 512 interrupt signals required attention with the help of a special facility in B-register 123 in relatively few instructions. Switching between these control registers could be done rapidly and Interrupt control had priority of action over the other two but relatively little time was spent there since it only had to identify the source of interrupt and then hand back an action request to deal with it to the other control registers.

Hardware

At this time semiconductor technology utilising germanium was replacing thermionic devices with advantages in size and reliability. The search was on to get sufficiently fast, reliable discrete transistors to assemble with other components e.g. diodes, resistors, capacitors etc. to make computer logic gates.

Basically there were two types of transistor. One was called a graded base device. It was relatively cheap to make but to operate quickly it always had to have at least three volts between its emitter and collector even in the on condition. This was the type of transistor used to provide the bulk of the gating transistors in Atlas and was the Mullard OC170.

The other type of transistor was called the surface barrier transistor which could operate quickly both into and out of saturation which is a condition with only very low voltage between emitter and collector e.g. 0.1 volts. These devices were made by Philco in the USA and later by Plessey in the UK. However the manufacturing process was quite involved and as a result these transistors were very expensive. However there was the idea that when switched on with such a small voltage drop across them they might be used to transmit a signal in a similar way to a relay mechanical contact provided that the switching condition remained unaltered during the transmission. In a parallel adder there is a condition when a carry signal might have to be transmitted from the least significant digit to the most significant. If this is 40 stages for example then through a conventional

transistor gate the transmission time is 40 gate delays, i.e. quite some time. However there was a known logic design for a relay parallel adder, where certainly there is a long time to switch the relays all of which occur in parallel, but then when the contacts are all set the transmission time of the carry signal is only along the length of wire connecting the relays and through their metallic contacts, i.e. very fast. Could the surface barrier transistor provide the fast switching speed required and also fast carry transmission and could the small change in signal level at each stage be accommodated? The answer was yes and this was the type of fast adder/subtractor designed for use in Atlas and, at the time, was the fastest addition available. The transistors used were the SB240 and SN501, the latter having a higher power rating.

Other interesting circuit contributions were made in Atlas in particular to driving and receiving signals with 50 ohm coaxial cable where it was possible to provide an output signal of 2.5 volts from a 9ma drive signal. This was important since there were many bundles of 25 or 50 coaxial cables to transfer signals between separate cabinets and also within cabinets. There was also a peak sense circuit using an electrical delay line which was used to identify the signals received from the magnetic tape and also the magnetic drum systems.

Progress and Problems in Producing Atlas

Professor Lavington in his recent article in *Resurrection 61* entitled *Atlas in Context* has referred to the national interest in developing a high performance computer from early 1957 which arose from the interest of NRDC and the perceived needs of the UKAEA and provides more detail about that situation. However some brief comments follow on the action which took place. A working party was set up and on the 17th March 1958 they visited the Computer Science Department at the University of Manchester to see the independent work there called Muse under the direction of Professor Tom Kilburn. In May they concluded that though the design seemed sufficiently fast they were unhappy with the main storage facilities and the lack of consideration about handling peripheral equipment. They also felt considerable more design effort was needed and expressed concern about the size of the team to do the job even with the help of Ferranti. These comments indicating lack of support were disappointing for the University team but later that year Ferranti decided to develop a computer based on the Muse design and it was then called Atlas. For the Muse team it was fantastic news.

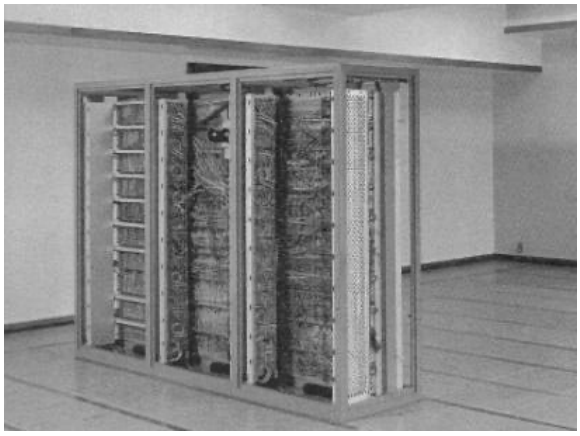
The first formal progress meeting on Atlas took place at the West Gorton factory on the 9th November 1959 and it was chaired by Peter Hall the Ferranti Computer manager accompanied by senior staff, Gordon Scarrott and Keith Lonsdale. Tom Kilburn and Dai Edwards attended on behalf of the University and these meetings occurred thereafter at monthly intervals on the second Monday every month until the project was complete. Kilburn outlined the work going on for Muse and Lonsdale described activity on peripherals for the Orion computer and what of this work could be common or at least adaptable for use on Atlas. It was agreed that Muse should now be called the Pilot Atlas and that work should continue to develop it including the connection of magnetic drums and magnetic tape. This development activity continued until February 1961 when the Pilot Atlas was moved to the factory for training purposes and this allowed the University computer room to be refurbished in time for the delivery of the first part of the commercial Atlas in June 1961.

A section of the Pilot Atlas, with boxes attached to a Dexion frame and Gordon Haley, Ianto Warburton and Yao Chen working on the central processor.

Now going back a bit in time, in early 1960 effort on the project was increased by using the Plessey Company to provide the random access storage (RAM) and the B-store, the Lancashire Dynamo company to provide the power supply and power switching facility and Ferranti Edinburgh to explore the provision of suitable magnetic tape decks from external suppliers. These tape decks were to be common to both the Atlas and Orion computers. All this work was leading edge activity, not straightforward production and some members of the Atlas team were closely involved in these activities; Mike Lanigan with storage, Gordon Haley with the power supply, David Aspinall with the magnetic tape and me with involvement in all three. Naturally there were problems with all these activities but all were solved in an acceptable time.

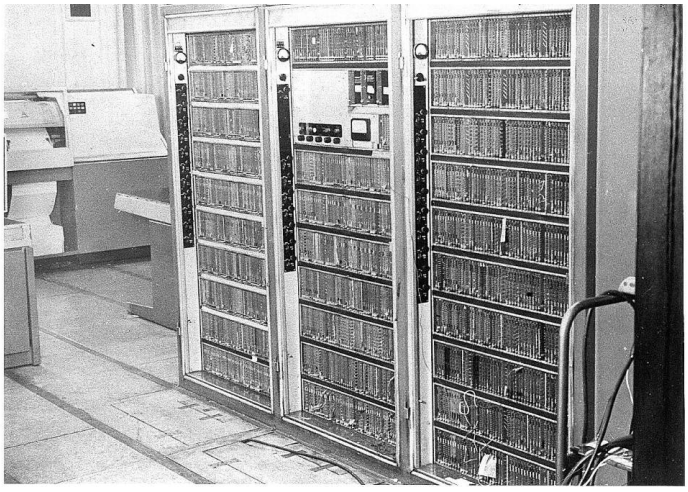
However there was a problem with the design of the magnetic drums and also the magnetic reading/writing heads which were the responsibility of Ferranti at West Gorton. The heads were to be identical for Atlas and Orion drums but the Atlas drum was to be a development on the Orion drum to run at higher speed — about 4750 rpm, and to have read write facilities from/to 24 tracks in parallel. Eric Dunstan of the Atlas team was responsible for the electronic design together with me and there was liaison with West Gorton to discuss the problems experienced which were essentially mechanical in nature but also involved adequate cooling too. Correction of these was a Ferranti responsibility and a number of improvements were made but the drums still did not operate to the order of reliability required, e.g. there were only two drums operational at the inauguration and not the four specified. These original drums were supplied to both the Manchester and London Atlas but were then replaced by Bryant drums to achieve satisfactory performance for both computers by late 1963. With hindsight this change should have been made much earlier.

The central processor bay on its way from the Ferranti factory to The University of Manchester in June 1961.



Now installed in the newly refurbished computer room which had previously housed the Ferranti Mark I and then the Pilot Atlas.

The back of the racks are visible in the photograph above showing the interconnection wiring and it is worthwhile here identifying the scale of the constructional problem. In each rack there were 10 boxes to house printed circuit boards, a maximum of 48 boards per box and each board plugged in to a 32 pin socket. Some of these pins, say five, are for power connections and were linked together on the box via bus bars so they caused few problems. Also not all pins were required so assume that 25 pins remained to be wired, i.e. 25 times 48 per box equals 1200. With 10 boxes per rack and three racks per bay there were now 36,000pins to be connected per bay and Atlas comprised some six bays. All these connections had to be carried out by hand, needed to be done accurately and the joints made properly so that there was a clear need for checking the activity which was also made more difficult since the pin spacing was quite small. The work of connection and checking generally proceeded in successive stages until the job was complete. Unfortunately too all this work had to be repeated for each computer that was made. Compare and contrast this work with the current situation of making a complete computer including memory on a physically small chip where automation plays a large part and takes place in ultra clean conditions.



Here we see the front of the central processor bay at a much later date fully populated with printed circuit boards where the boxes housing the cards can now be seen clearly. In the centre rack two of the box positions were occupied by the B-store. To the left of the bay the lineprinter is evident and further left a small part of the unit on which the Atlas console is placed is just visible. The printed circuit cards were packed very closely and some problems arose from this because when a card was unplugged with the power still on then it was possible for the earthed metallic cover on the transistors of the board being unplugged to cause a short circuit to the printed circuit connections on the

back of the adjacent board. This problem was detected early and was solved by attaching a thin mica insulating sheet by plastic pins to the back of every board. Whilst this was effective it did make the job of the maintenance engineer a bit more tedious.

From June 1961 to August 1962 various pieces of Atlas were delivered and commissioned: the random access store was the last. From September 1962 Atlas started to become usable for significant periods of time. Most of the equipment was there for the inauguration in December except for some drums and peripheral equipment, for example the lineprinter which was held up by fog in Idlewild Airport.

After the inauguration various hardware developments occurred — offline data links to Edinburgh and Nottingham Universities and also to Ferranti in London, online data links through privately contracted wires, the provision of a large capacity disc (< 100 Mbytes), a speech converter system and finally an instrument for use by X-ray crystallographers to collect data and then calculate the structure. However the critical effort to make Atlas really usable was the development of the Supervisor, the computer operating system in modern terminology. This took the best part of a full year to achieve its full potential but then the subsequent work done by the Harwell Atlas which was the biggest Atlas was immense. However that is another complete story in itself.[2] [3]

The University of Manchester Atlas was shut down on the 30th September 1971 having provided a good computing service to the University, some other Universities too and also to Ferranti who utilised 50% of the total time available. The photograph below shows a representative group of people involved in the Atlas development and use, in front of the Atlas console. From the left Bill Talbot, then ICL manager at West Gorton, Gordon Black, user and also new head of the Manchester Regional Computer Centre, Tom Kilburn seated, Gordon Haley, ICL engineer on Atlas, and Ken Midmer who was representing Sebastian de Ferranti on this occasion.

This is an edited version of the presentation made by Emeritus Professor Dai Edwards at the 50th Anniversary of the Atlas Computer at the University of Manchester on 5th December 2012. Contact at dbgedwards@boundlessmail.com.

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[2] *The Atlas Supervisor, Kilburn, Payne and Howarth. 20th Proceedings of the 1961 Eastern Joint Computer Conference*
[3] *Evaluation of Operating Systems Brinch Hansen 2000 CiteSeerX pages 7&8*